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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/602,901	06/23/2000	James R. Peterson	500689.01	9313

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	13

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/602,901	Applicant(s) PETERSON ET AL.	
	Examiner Hau H Nguyen	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *1,8,14,19,26 and 31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9-13,15-18,20-25,27-30 and 32-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2-7, 9-13, 15-18, 20-25, 27-30, and 32-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (U.S. Patent No. 6,252,612) in view of Cox (U.S. Patent No. 5,357,621).

Referring to claims 4, 10, 16, 35, 37, as shown in Fig. 2, Jeddeloh teach a computer 150 includes at least one processor 152 connected to a first memory controller 154 and a second memory controller 155 by a processor or host bus. The computer 150 also has a first main memory 156 and a second main memory 157 connected to the first memory controller 154 and the second memory controller 155, respectively (col. 4, lines 5-12). As also shown in Fig. 2, the first memory controller 154 and the second memory controller 155 are coupled through a bus 153. With reference to Fig. 3, Jeddeloh further teaches the first memory controller 154 provides a set of registers to define the range of available for AGP transactions. A base register 165 is used to define the base address of the AGP addresses. A range register 166 is used to establish the amount of memory following the base address that is dedicated to AGP transactions (col. 4, lines 59-64). Using the base 165 and range 166 registers provided by the first memory controller 154, the operating system has set the AGP related data occupying the lower 32 megabytes of the first

main memory 156 referenced by physical addresses 0x00000000 through 0x01FFFFFF (segmented memory array). Jeddeloh also teaches upon a request from the graphics accelerator 160 the first memory controller 154 analyzes the address in the request to identify whether the address is in the first main memory 156. If the address is not within the first main memory 156, the first memory controller 154 re-routes the request to the second memory controller 155 (col. 5, lines 17-42).

Thus, Jeddeloh teaches all the limitations of claim 4, except that faulty memory sub-arrays is left unassigned.

However, Cox teaches a memory system network consists of a central memory system controller and at least one individually addressable memory module controller coupled serially to the memory system controller. Various command signals generated by the memory system controller and information or data signals generated either by the memory system controller or individual memory module controllers in response to commands transmitted from the system controller, are transmitted and received serially between the system controller and the memory module controllers (col. 2, lines 36-50). The expandable memory system utilizes a plurality of plug-in, add-on memory modules or memory cards wherein each individual memory module comprises a module controller, a module memory address control logic block and at least one memory block having a number of individually addressable memory cells (memory sub-array) (col. 2, lines 53-59, also with reference to Fig. 1). Cox also teach the system includes the capability to bypass or disable bad memory modules and reassign memory addresses without leaving useable memory unallocated (col. 3, lines 37-39).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Cox in combination with the method as taught by Jeddeloh in order to provide a contiguous memory (col. 5, lines 26-29).

Referring to claims 2, 9, 15, 17, 34, Jeddeloh teach the memory controllers may be on the same semiconductor chip as the memory that they control (col. 8, lines 8-10).

In regard to claims 3, 5, 11, 18, 32-33, 39, Jeddeloh teaches the first memory controller 154 provides a set of registers to define the range of available for AGP transactions. A base register 165 is used to define the base address of the AGP addresses. A range register 166 is used to establish the amount of memory following the base address that is dedicated to AGP transactions (col. 4, lines 59-64). As cited above, Cox teaches the memory system capable of bypassing or disabling faulty memory and reassigning memory addresses. It is implied that the memory system as taught by Cox should be able to keep track of the number of functional memory blocks, because otherwise, access to memory would be misallocated.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Cox in combination with the method as taught by Jeddeloh in order provide a contiguous memory (col. 5, lines 26-29).

In regard to claims 6-7, 12-13, 36, 38, as shown in Fig. 3 and as cited above, Jeddeloh teaches the first memory controller is assigned 32 megabytes of memory starting from 0x00000000 through 0x01FFFFFF (hexadecimal), and the second memory controller is assigned 32 megabytes of memory starting from 0x02000000 through 0x03FFFFFF, that means the starting address of the second memory controller is the sum of the start value and the size value of the first memory controller.

Referring to claims 22 and 28, Jeddeloh teaches a computer, comprising at least one processor; and at least two memory controllers, wherein one of the at least two memory controllers includes an accelerated graphics port and at least one configuration register defining a range of addresses that are available for accelerated graphics port transactions (col. 3, lines 36-42). As shown in Fig. 2, Jeddeloh teaches the computer 150 includes at least one processor 152 connected to a first memory controller 154 and a second memory controller 155 by a processor or host bus. The computer 150 also has a first main memory 156 and a second main memory 157 connected to the first memory controller 154 and the second memory controller 155, respectively. A graphics accelerator 160 communicates with a local frame buffer 162 and the first memory controller 154 through an accelerated graphics port (AGP) 166. The AGP 166 is a point-to-point connection between the first memory controller 154 and the graphics accelerator 160 (col. 4, lines 5-26). It is inherent that the computer system of Jeddeloh should include a system processor, a system bus, and a display logic to drive a display.

As cited above, with reference to Fig. 3, Jeddeloh further teaches the first memory controller 154 provides a set of registers to define the range of available for AGP transactions. A base register 165 is used to define the base address of the AGP addresses. A range register 166 is used to establish the amount of memory following the base address that is dedicated to AGP transactions (col. 4, lines 59-64). Using the base 165 and range 166 registers provided by the first memory controller 154, the operating system has set the AGP related data occupying the lower 32 megabytes of the first main memory 156 referenced by physical addresses 0x00000000 through 0x01FFFFFF (segmented memory array). Jeddeloh also teaches upon a request from the graphics accelerator 160 the first memory controller 154 analyzes the address in the request to

identify whether the address is in the first main memory 156. If the address is not within the first main memory 156, the first memory controller 154 re-routes the request to the second memory controller 155 (col. 5, lines 17-42).

Thus, Jeddeloh teaches all the limitations of claims 22 and 28, except that faulty memory sub-arrays is left unassigned.

However, Cox teaches a memory system network consists of a central memory system controller and at least one individually addressable memory module controller coupled serially to the memory system controller. Various command signals generated by the memory system controller and information or data signals generated either by the memory system controller or individual memory module controllers in response to commands transmitted from the system controller, are transmitted and received serially between the system controller and the memory module controllers (col. 2, lines 36-50). The expandable memory system utilizes a plurality of plug-in, add-on memory modules or memory cards wherein each individual memory module comprises a module controller, a module memory address control logic block and at least one memory block having a number of individually addressable memory cells (memory sub-array) (col. 2, lines 53-59, also with reference to Fig. 1). Cox also teach the system includes the capability to bypass or disable bad memory modules and reassign memory addresses without leaving useable memory unallocated (col. 3, lines 37-39).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Cox in combination with the method as taught by Jeddeloh in order to provide a contiguous memory (col. 5, lines 26-29).

Referring to claims 20, 27, and 29, Jeddeloh teach the memory controllers may be on the same semiconductor chip as the memory that they control (col. 8, lines 8-10).

In regard to claims 21, 23, and 30, Jeddeloh teaches the first memory controller 154 provides a set of registers to define the range of available for AGP transactions. A base register 165 is used to define the base address of the AGP addresses. A range register 166 is used to establish the amount of memory following the base address that is dedicated to AGP transactions (col. 4, lines 59-64). As cited above, Cox teaches the memory system capable of bypassing or disabling faulty memory and reassigning memory addresses. It is implied that the memory system as taught by Cox should be able to keep track of the number of functional memory blocks, because otherwise, access to memory would be misallocated.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Cox in combination with the method as taught by Jeddeloh in order provide a contiguous memory (col. 5, lines 26-29).

In regard to claims 24-25, as shown in Fig. 3 and as cited above, Jeddeloh teaches the first memory controller is assigned 32 megabytes of memory starting from 0x00000000 through 0x01FFFFFF (hexadecimal), and the second memory controller is assigned 32 megabytes of memory starting from 0x02000000 through 0x03FFFFFF, that means the starting address of the second memory controller is the sum of the start value and the size value of the first memory controller.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

04/28/2004

Matthew C. Bella

MATTHEW C. BELLA
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